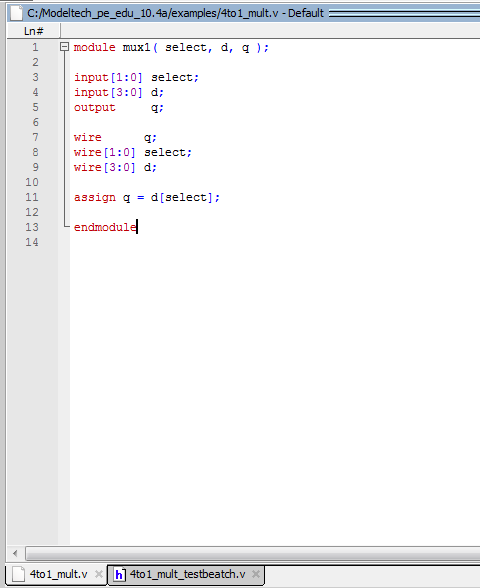
Chirag solanki

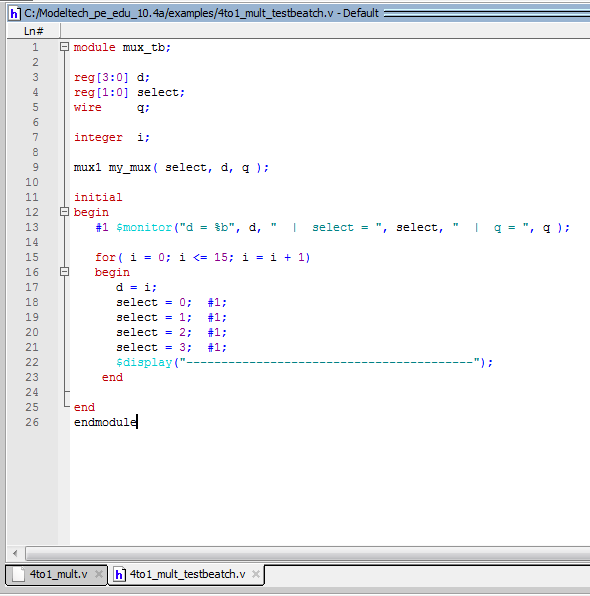
15035

Homework assignment 4

Answer 4



Test batch



Answer 5

*module mux(a,b,c,d,e,sel,out);*

*input a,b,c,d,e;*

*input[2:0] sel;*

*output out;*

*reg out*

always @(in0 or in1 or in2 or in3 or in4 or in5 or sel)

case (sel)

3’b000 : out = in0;

3’b001 : out = in1;

3’b010 : out = in2;

3’b011 : out = in3;

3’b100 : out = in4;

3’b101 : out = in5;

default : out = 64’bz;

endcase